In LSI failure analysis, the electron beam absorbed current method is becoming widely used as a technique for localizing open/short failure in LSI-interconnects. This paper reports several results where this method was used for the LSI failure analysis and some knowledge of usage which was acquired through these studies.

**Keywords**: Failure Analysis, Electron Beam Absorbed Current, LSI-interconnects, Failure localization.

### Introduction

With recent shrinking of feature size and increasing number of metal layers in integrated circuits, determination of the physical root cause by failure analysis is becoming extremely difficult. Especially, due to the multi-layered structures, the case of the failure factor existing in dielectric layer such as Via that connect two metal layers has been increased. In this case, localization of failure site by the layer analysis (Top-Down surface observation for each layer) seldom reaches to the physical root cause, thus cross-sectional observation is required. For cross-sectional observation, improvement of accuracy for precise failure site localization, where a cross-sectional imaging and analysis should be performed, leads to the improvement of determination for physical root cause.

As a method for localizing open/short site in LSI-interconnects, utilizing electron beam ability for focusing, transmission and absorption, the advantage of Resistive Contrast Imaging (RCI) has been reported. In Japan, this method is called "Electron Beam Absorbed Current method." Thus, in this paper, we describe this method as the Electron Beam Absorbed Current method [1-8].

In this paper, using a JEOL Beam Tracer, authors report the results of application of the Electron Beam Absorbed Current method to localize LSI failure sites and some knowledge of usage acquired through our study.

### Flowcharts for Localizing Failure Sites

In localizing the LSI failure sites, suitable methods are applied depending on failure modes. In general, for DC failure, Optical Beam Induced Resistance Change (OBIRCH) and an emission microscope, for SCAN failure, a software diagnosis tool, for function failure other than SCAN failure, an emission microscope and for memory failure, a fail-bitmap technique are used. In recent years, Dynamic Laser Stimulation (DLS) analysis has started to be used for localizing AC failure [9], [10]. These techniques and tools enable us to localize the failure site from the entire chip level down to the functional block and cell level. A rough guideline for the area of localization using these methods is about a 100 µm square. However, to perform a cross-sectional observation, the area of localization should be achieved at least down to a 100 nm square. For example, in case of LSI interconnects failure, it is necessary to localize accurate failure sites along interconnect with 100 nm width, or specify just one Via that connects interconnects fixed in different layers. In case of cell failure, it is necessary to specify one defective transistor within multiple transistors.

**Figure 1** shows the flowcharts for localizing failure sites down to 100 nm square range. For interconnects failure, the Electron Beam Absorbed Current method is used, and for cell failure, Nano-probing analysis is applied.

### Analysis Examples Using Electron Beam Absorbed Current Method

Some examples using the Electron Beam Absorbed Current method in Fig.1 are demonstrated to localize AC contacts and short-failure in LSI-interconnects.

**Short-failure in LSI interconnects**

**Figure 2** shows an analysis example of function failure in a half-pitch(hp) 130 nm System on a Chip (SoC) product. The analysis result using an emission microscope indicated two anomalous emissions on the chip. Then, the interconnect that connects with each cell at an anomalous emission site was referred with layout diagram. Then it was found that the total length of this interconnect was 3 mm and also, the target analysis area was spread to a wide area of 1.25 mm × 0.65 mm. In this analysis, the Electron Beam Absorbed Current method was used to localize the area down to a 100 µm square, so that physical analysis can be performed. As a result, an extra interconnect, which is different from defective interconnect was detected on an absorbed current image. This result suggested that a short-site exists on the defective interconnect. The absorbed current image and the short candidate site on layout data are shown on **Fig 3**.

The layer analysis was performed till the top surface of Al interconnect for the short candidate site, but no abnormal phenomenon was observed. However, the absorbed current image suggested a high possibility of the existence of a failure in this site. Thus, we polished the Al interconnect but left barrier metal and observed the layer again. As a result, a particle at the bottom of barrier metal on M3 layer was identified as a cause of the shortage. The results of layer analysis were shown on **Fig 4**. Generally, layer analysis was not performed in such detailed observation. But in this case, a failure site was successfully localized to an area of about 5 µm × 1 µm by an absorbed current image. Thus, we concentrated on analyzing this area, and then the physical root cause of the failure was determined.

**High resistance failure in Via**

Analysis example of AC failure in an hp 90 nm SoC product is described here. This failure is a temperature-dependent SCAN failure. We localized a failure site using the flowchart...
Fig. 1 Flowcharts for localizing failures sites.

Fig. 2 Short candidate interconnect.

Fig. 3 Absorbed current image and short candidate.
Reflection protective film
Polished till here and observed.
Al interconnect
Barrier metal
Particle
Polishing Al interconnect
Further polished till here and observed.
Al interconnect was eliminated by polishing.
Particle was identified under Al interconnect.
Cross-sectional TEM image
Barrier metal
600nm
Particle was finally observed by leaving barrier metal under Al interconnect.
Cross-sectional TEM

**Flowchart for localization**

- Software diagnosis tool
  - Localizing defective Path
  - Localizing defective node
- DLS analysis
  - Localizing defective node
- Localizing failure site
- Circuit simulator
  - Estimating failure site and resistance
- Nano-probing analysis
  - Resistance measurement
- Absorbed current image analysis
  - Localizing failure site
- Physical analysis (cross-sectional TEM observation)
  - Failure confirmation

**Fig. 4 Results of layer analysis.**

In this example, all results from various analysis tools were in good agreement, so it was said that the accuracy of the localization was sufficiently high. Also, it was found that the Electron Beam Absorbed Current method could give useful information for failure localization.

**Low resistance failure in Via**

Figure 8 shows an analysis example of function failure on an hp 90 nm SoC product. In this example, an emission microscope analysis detected anomalous emission and this result suggested an open failure in the interconnect between the cell and the emission site. As a result, cross-sectional TEM observation indicated open Via in this interconnect. However, in the process of the localizing, an increased to several million Ω. After this confirmation, the resistance of this interconnect was measured with a Nano-probing technique. From this Nano-probing measurement, it was confirmed that the resistance at room temperature was about 12 MΩ and that at high temperature was about 300 Ω. These resistances corresponded to the results of simulations. Furthermore, from the absorbed current image of this interconnect, the contrast of defective interconnect was changed in the site shown in Fig. 7. This result also corresponded to the DLS analysis. As a result of comparing with layout diagram, it was revealed that Via exists in this site. Then, a cross-sectional observation of this Via was performed, indicating that a void exists in the Via. This void was considered to be caused during filling process of the hole.

Since this failure has a temperature dependence, Dynamic Laser Stimulation (DLS) was applied to a candidate of defective interconnect and node, both of which were extracted from a software diagnosis tool. (Although DLS is generally referred to Soft Defect Localization (SDL), we call DLS in this paper.) DLS result and a superimposed image of a defective node with DLS mapping are shown in **Fig. 6**. This result indicated that the DLS sensitive area exists on the node extracted from the software diagnosis tool, so the failure site was highly assumed to be in this area.

On a circuit simulator, we increased the resistance at failure candidate site with several times, and simulations were carried out. Then the reproducibility of the failure phenomenon had been confirmed when a resistance increased to several million Ω. After this confirmation, the resistance of this interconnect was measured with a Nano-probing technique. From this Nano-probing measurement, it was confirmed that the resistance at room temperature was about 12 MΩ and that at high temperature was about 300 Ω. These resistances corresponded to the results of simulations. Furthermore, from the absorbed current image of this interconnect, the contrast of defective interconnect was changed in the site shown in Fig. 7. This result also corresponded to the DLS analysis. As a result of comparing with layout diagram, it was revealed that Via exists in this site. Then, a cross-sectional observation of this Via was performed, indicating that a void exists in the Via. This void was considered to be caused during filling process of the hole.

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suggests that a resistance at this point should be relatively low.

To detect such a low-resistance failure site using the Electron Beam Absorbed Current method, we found that a lower primary electron beam current was required. Figure 9 shows the variations of absorbed current images when the probe current was set to 36 pA and 530 pA while the accelerating voltage was varied from 10 kV, 13 kV, to 15 kV. In the case of a probe current of 530 pA, regardless of the accelerating voltage (10 kV, 13 kV, 15 kV), whole interconnect appeared on the images. On the other hand, in case of a probe current of 36 pA, the boundary of the contrast at the failure site was recognized at an accelerating voltage of 10 kV. However, when the accelerating voltage was increased to 13 kV and 15 kV, it became difficult to recognize the boundary at the failure site. In Fig.8, although the interconnects are located on the same fourth metal layer (M4), the absorbed current image showed a featureless dark contrast. Thus, the open failure is expected to exist on the Via between the interconnects on the fifth metal layer (M5).

This result indicates that, in order to detect a low-resistance open failure, it is necessary to reduce the probe current and the accelerating voltage. However, by suppressing the probe current and the accelerating voltage, the image contrast becomes poor, so to increase the detection rate of low-resistance open failure and to get fare contrast of the image are a trade-off relation. In general, in order to improve the image contrast, the probe current and the accelerating voltage are set relatively higher. However, when the prioritizing the
prevention of improper contrast at the low-resistance open failure, it is necessary to start observation from lower probe current and lower accelerating voltage to higher.

On this sample, observation by two probes method was also performed. Figure 10 shows absorbed current images obtained with one probe and two probes, respectively. In the case of one probe, whole interconnects are appeared on the image at a probe current of 36 pA and 500 pA. No boundary of the contrast is recognized at the open failure site. On the other hand, in case of two probes, a clear boundary of the contrast appears at the open failure site at both 36 pA and 500 pA. This result demonstrates that when two probes method is available, the low-resistance open failure can be detected regardless of high and low probe current.

Discussion on an undetectable low-resistance open failure

In the present study, when one probe was used for detecting the absorbed current, some results showed that whole interconnects were seen as the absorbed current image even if these interconnects contained a low-resistance open failure. This will lead to the misunderstanding of failure localization process in LSI failure analysis. Thus, in order to prevent misunderstanding of failure sites localization process, we made a physical model for this phenomenon and obtained the optimum observation conditions.

Figure 11 shows the equivalent circuits for device, where an Electron Beam Absorbed Current method was applied. In addition, Fig. 11 also shows the total equivalent circuit including an electron microscope, which was considered to be the corresponding power supply. When the probe current is 36 pA, the boundary of the contrast along the interconnect appeared and disappeared depending on the value of accelerating voltage. To keep constant probe current of 36 pA, when the voltage of power supply (accelerating voltage) changes, the output impedance Z of the power supply needs to be changed. When the probe current is 36 pA and an accelerating voltage is 10 kV, that is the condition of \( Z \ll R \), low-resistance open failure site can be observed. Here, \( R \) denotes the resistance at failure site. And when the probe current is 36 pA and an accelerating voltage is set to 13 kV or more, that is the condition of \( Z \gg R \), low-resistance open failure site cannot be observed. This model is considered to hold even for the case where the probe current is changed at a
The limitations are undetectable. In observation by two probes, one probe is set to observe the absorbing current image. However, when the impedance Z is high, there will be improper detection in failure sites. Further examination and experimentation will be expected in this future model equation.

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This model equation for impedance Z of the power supply is described below.

\[ Z = a \times \text{(accelerating voltage)} \times \text{Ip} \]

Further examination and experiment will be expected in the future for this model equation.

In observation by two probes, one probe is connected to ground potential. Thus, no matter how high the impedance Z is, a failure site is recognized in the absorbed current image. But in the failure analysis for actual devices, limitations of the layout prevent us from using two probes method. So, about 90 percent or more of the devices, only one probe observation can be allowed. In Fig. 12, the limitations are listed for observation by two probes.

In the case of observation by one probe, in order to prevent improper detection of a low-resistance open failure site, it is necessary to set the accelerating voltage and the probe current to lower values.

**Conclusion**

The Electron Beam Absorbed Current method was applied to the localization of failure sites of actual devices, and the following knowledge was acquired.

1. By combining a software diagnosis tool, an emission microscope and DLS with the absorbed current image, AC failure sites can be localized. The Electron Beam Absorbed Current method can give useful information for improvement of the accuracy to localize failure sites.
2. In observation by one probe, the absorbed current image may cause improper detection of failure sites under some observation conditions.

Based on the knowledge acquired from this study, we will clarify the model that explains the conditions for improper detection in observation by one probe. And furthermore, we will examine detectable resistance in LSI interconnects.

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**References**


